matthew

D3.1

Report on active transmission technology

Project number:	610436
Project acronym:	MATTHEW
Project title:	MATTHEW: Multi-entity-security using active Transmission Technology for improved Handling of Exportable security credentials Without privacy restrictions
Start date of the project:	1st November, 2013
Duration:	36 months
Programme:	FP7-ICT-2013-10

Deliverable type:	Report
Deliverable reference number:	ICT-610436 / D3.1
Activity and Work package contributing to the deliverable:	WP 3
Due date:	November 2014 – M13
Actual submission date:	November 29th 2014

Responsible organisation:	AMS
Editor:	AMS – Giuliano Manzi
Dissemination level:	Public
Revision:	1.0

Abstract:	This document describes the key feature and basic operational principle of an active transmission technology based system. It includes description of Transmission subsystem, Receiver subsystem and interface mechanism with Secure Elements. Further Keywords: Include description of special feature planned to be unique feature ad-hoc designed according to the Matthew project system specification.
Keywords:	MATTHEW, active transmission technology, IC system architecture.

This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 610436.

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Executive Summary

In the last 10 years, contactless technology has been getting more and more interest in the smart card industry and has moved from a very proprietary piece of technology to a more and more standardized technology with ISO/IEC14443 and Near Field Technology (NFC). With NFC, this technology has also moved out of the pure smart card world, going into a variety of form factors and different type of devices.

The key problem though faced by industrial actors has been the constraints the core foundation of contactless smart card relies on: magnetic field coupling. Key constraints have therefore been the need to have big antennae that limit miniaturization and to avoid conducting materials which basically 'sink' the magnetic field. In the last 2 to 3 years, a new piece of technology called active transmission or active load modulation (ALM) has been coming to market addressing some of the limitations of traditional RFID, specially the limitation on the size of the antenna.

This report starts by outlining the functioning principles of active transmission technology and the reasons why it enables miniaturized antenna for devices like microSD or SIM cards which are not possible with tradition contactless card technology which relies on passive load modulation.

A high level description of the key building blocks of the active transmission RF front end in development for Matthew prototyping activities and their respective roles is provided.

The last two sections of this report go more in details and provides an outline the new technologies studied and prototyped as part of the Matthew project that are not available in state and commercial active transmission products available today.

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Chapter 1 Introduction

Purpose of this report is to describe the functioning of the Active Load Modulation (ALM) front-end, called AS3924, which ams AG is working on in the context of Matthew project.

When the Matthew project was applied for, ams AG was finalizing the development of its first product called AS3922 which has been implemented in some products available on the market today. Since the Matthew project application, ams AG has developed another product called AS39230 which is designed to be connected to an NFC controller which is not the scope of Matthew project. The AS3924 which ams AG is working on in the context of Matthew project aims at implementing a significant amount of improvements in comparison to AS3922 to address the requirements identified for Matthew: high baudrates, improved modulation techniques to enhance even more the performance of small antennae.

Chapter 2 Technical Description

The AS3924 is an advanced NFC active contactless card front-end with “Active Boost” technology. Compared to its predecessor AS3922, will provide improved performance and several new features.

It is designed for environments that require HF contactless card functionality, where systems with passive load modulation are challenged. In combination with a standard secure element, AS3924 is ideal for implementing a payment device in the form factor of a SIM, a microSD or micro/nanoSIM, or an embedded secure element.

Active Boost technology generates a contactless card response by actively transmitting a signal which is synchronous to the reader field allowing for reader to card communication one order of magnitude lower than conventional passive load modulation allows.

The AS3924 leverages ams’ unique antenna auto tuning (AAT) and automatic power control (APC) technologies. These give the AS3924 unrivalled performance in challenging, dynamic environments prevalent in typical SIM or microSD/SIM mobile applications.

The AS3924 is compliant to ISO14443 and FeliCa protocols. For easier integration into current systems the AS3924 can interface directly to a contactless interface of existing secure elements (SE) via Advanced ContactLess Bridge (ACLB) or Near Field Communications Wired Interface (NFC-WI, defined in ISO/IEC 28361) interfaces.

2.1 Active transmission (or Active Load Modulation ALM) technology principles

With passive traditional HF contactless cards the communication from PICC back to the reader (PCD) occurs by mean of passive load modulation.

The basic components of a contactless system are the contactless reader or Proximity Coupling Device (PCD) and a transponder or Proximity IC Card (PICC).

The PCD is an antenna connected to an electronic circuit. The PICC consists of an inductive antenna and an integrated circuit connected to the ends of the antenna. The combination PCD–PICC behaves like a transformer. An alternating current passes through a primary coil (PCD antenna) and creates an electromagnetic field, which induces a current in the secondary coil (PICC antenna). The PICC converts the electromagnetic field (or RF field) transmitted by the PCD, into a DC voltage by means of a diode rectifier to power the PICC’s internal circuits.

Load modulation is based on the electromagnetic coupling (i.e. Mutual inductance) between PICC and PCD similar to the power transfer and communication from PCD to PICC. The PICC changes the current in its antenna by switching on and off a load connected to the antenna. The current variation in the PICC antenna is sensed by the PCD as a small change in the current in its antenna, typically sensed as a small increase in voltage across a resistor in series with the PCD antenna.

The configuration and tuning of both antennas determines the coupling efficiency from one device to the other. In passive system the coupling factor between the reader and the card antennae is limited by the size of the antenna of the cards.

To overcome those limitations the active transmission technology actively drives the current in the antenna in phase with reader HF carrier signal. This is illustrated on Figure 1where the super-imposition of the answer on the reader coil is shown.

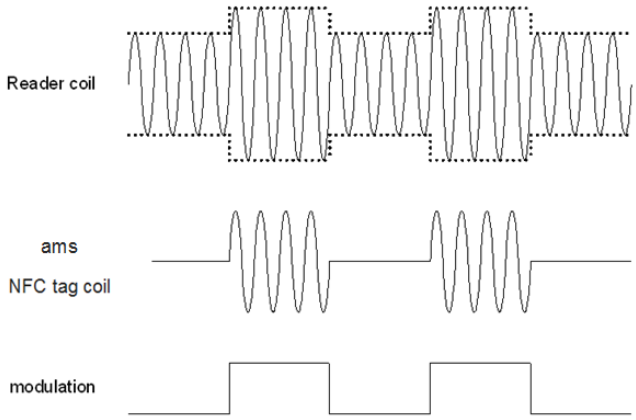

Figure 1: Active transmission wave shapes examples

2.2 AS3924 Protocol related features

- ISO14443 (A&B) and FeliCa up to 424 kb/s card with active transmission
- Internal timing defined by VCO locked to reader frequency
- Delay compensation and synchronization to assure transmission in phase with reader field
- ACLB and NFC-WI interfaces for communication to SE
- Power supply switch for SE
- Built in EEPROM for operating option settings
- SPI interface and interrupt signal for communication with host controller
- XOR TX modes for BPSK and FeliCa
- Multiprotocol mode
- System parameters exchange over ACLB
- Additional SE supply switch
- Separate supply pin for digital IO signals (range 1.62V to 3.6V)
- 2 wire SPI interface

2.3 AS3924 energy efficiency-related features

- Low impedance output driver with adjustable output power
  - Supply voltage range from 2.7V to 3.6V
  - Reduced antenna driver output resistance to 2Ω
  - Dedicated low power wake up mode
  - Frequency check during wake-up

2.4 AS3924 Special features

- Automatic Antenna Tuning through control of external variable capacitor
- Additional pins for antenna LC tank damping
- Integrated diagnostics system (IC self-test)
- XOR mode for all ISO modes
- VCO and RCO auto-calibration

Chapter 3 System overview

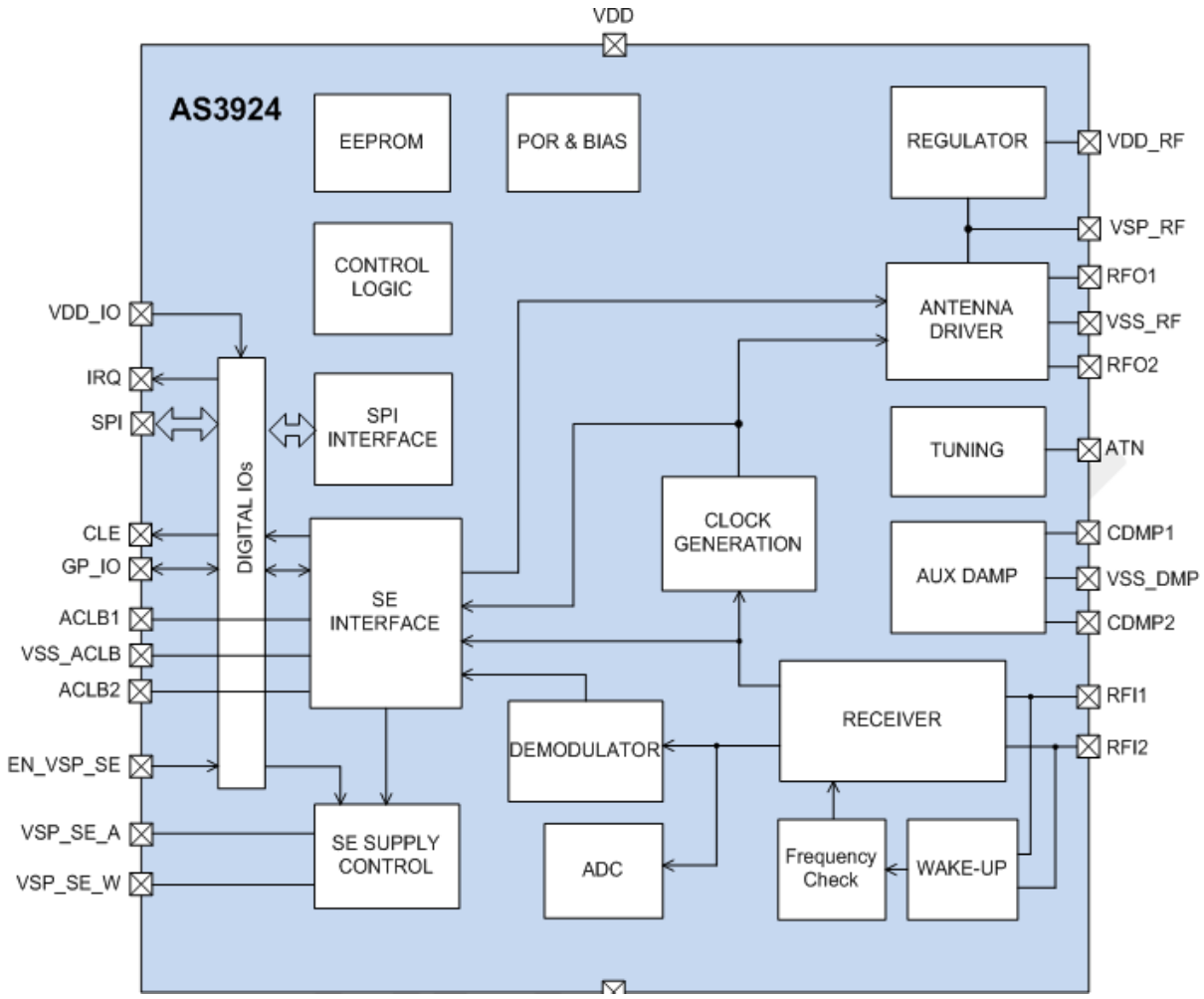

Figure 2: AS3924 Block Diagram

3.1 Tx Subsystem

3.1.1 Antenna Driver

This block contains two low impedance differential push-pull drivers which drive the antenna LC tank. In differential mode the drivers are driven in counter phase, in single mode they are driven synchronously, so in case they are connected externally in parallel lower output impedance is achieved.

3.1.2 Regulator

This block is used to control the antenna driver output power. It provides regulated voltage which supplies Antenna Driver output stage. Driver output power can be controlled through feedback loop which changes regulated voltage depending on input signal level. This regulator is also used to reduce output power during AAT and system diagnostic measurements.

3.1.3 Tuning system

Automatic Antenna Tuning (AAT) is performed by providing an analog output pin ATN which controls external voltage controlled capacitor.

3.1.4 AUX damp system

This block supports additional damping of oscillation on the antenna LC tank which is needed in certain applications to implement BPSK and FeliCa card to reader communication.

3.2 Rx Subsystem

3.2.1 Receiver

This block amplifies the input signal, provides the clock signal which is extracted from the reader carrier frequency, and generates a signal which is proportional to the input signal amplitude. It provides the following functionality:

- input signal conditioning
- variable gain with AGC (AGC includes also attenuation)
- clock extraction
- peak detector (rectification)
- interface activation

3.2.2 Clock Generator

This block contains a PLL and an auxiliary RC oscillator.

During reception, the PLL is locked to the extracted clock. When the TX driver is active, the clock extractor output does not contain information about reader field; therefore, the PLL feedback loop is opened and the VCO continues to run with the phase that was established while PLL was locked.

By calibrating RC oscillator time constants used in receiver and demodulator are adjusted. When needed it is also used to provide auxiliary clock signal.

This block also contains a phase adjustment block, which adjusts the phase difference between RFI and RFO signals.

3.2.3 Demodulator

This block detects modulation superimposed on the reader carrier signal which is used for reader to card communication.

3.2.4 ADC

Analog to digital converter is used to provide digital information about the amplitude of the input signal. This information is used in AAT procedure and for different system purposes.

3.2.5 Wake-up system

The Wake-up block is used to detect presence of signal produced by the reader field on RFI1 and RFI2 inputs. Detection of signal on RFI inputs enables the frequency check block. The wake-up threshold is adjustable.

3.2.6 Frequency check block

In case input signal which has triggered Wake-up block is in a frequency band around 13.56 MHz operation of other blocks is enabled. This new block reduces current consumption in case of presence of noise and perturbations.

3.3 Digital and Interface Subsystems

3.3.1 SE data interface and power supply

This block interfaces external secure elements (SE) supporting either interface to SE having contactless (CL) interface or NFC-WI interface.

Interface to SE having CL interface is called ACLB. It is designed to support a contactless interface with maximum resonance capacitor of 30pF. The ACLB interface contains two configurable push pull drivers. The push resistance to VDD is lower than pull resistance to VSS in order to avoid generating cross currents in the SE contactless interface.

The reader to card modulation signal extracted by the receiver controls the ACLB. In case of OOK modulation ACLB is blocked, in case of AM modulation the output level is reduced.

ACLB is constantly monitoring the level of signal on its outputs in order to detect a drop produced by SE modulator switch during card to reader communication. During modulated periods the driver is switched on.

The SE supply block provides two switch outputs which may be used to supply external SEs. Depending on configuration they may be automatically switched on when presence of reader field is detected, additionally the AS3924 can be configured to switch on SE supply when EN_VSP_SE is high. Input signal EN_VSP_SE can be put high by external controller whenever the SE element is accessed through ISO7816 bus. The two switches can also be directly controlled through SPI.

VSP_SE_A which is intended to supply the IC connected to ACLB interface is switching to VDD, while VSP_SE_W is intended for SE connected to NFC_WI interface and is switching to VDD_IO.

3.3.2 SPI communication interface

The controller controls the AS3924 operation and observes its internal state through the SPI interface. The controller has access to the internal registers and EEPROM.

3.3.3 Digital I/O

This block contains level shifters which allow use of VDD_IO supply level for communication over SPI and NFC-WI interfaces.

Chapter 4 Detailed System Description and Diagram

The AS3924 is an advanced contactless card emulation analog front end IC which produces the card to reader reply by active driving in the antenna a signal which is synchronous to the reader field. The AS3924 extracts the reader carrier signal and demodulates the reader to card modulation which is superimposed to it. The demodulated signal is sent to an external IC (usually secure element) through ACLB or NFC-WI interface. The external IC provides on the same interface a card to reader reply which is then actively transmitted by AS3924 Antenna Driver.

Figure 3 depicts a simplified system diagram of a typical AS3924 application including key AS3924 blocks. The AS3924 interfaces on one side antenna LC tank and on the other an IC with contactless card logic connected to either ACLB or NFC-WI interface. Since in most cases this IC is a Secure Element, the expression SE interface is used in this document for the interface block comprising ACLB and NFC-WI interfaces. Optionally a controller may be connected to the AS3924 SPI interface to control the operation and define operating options.

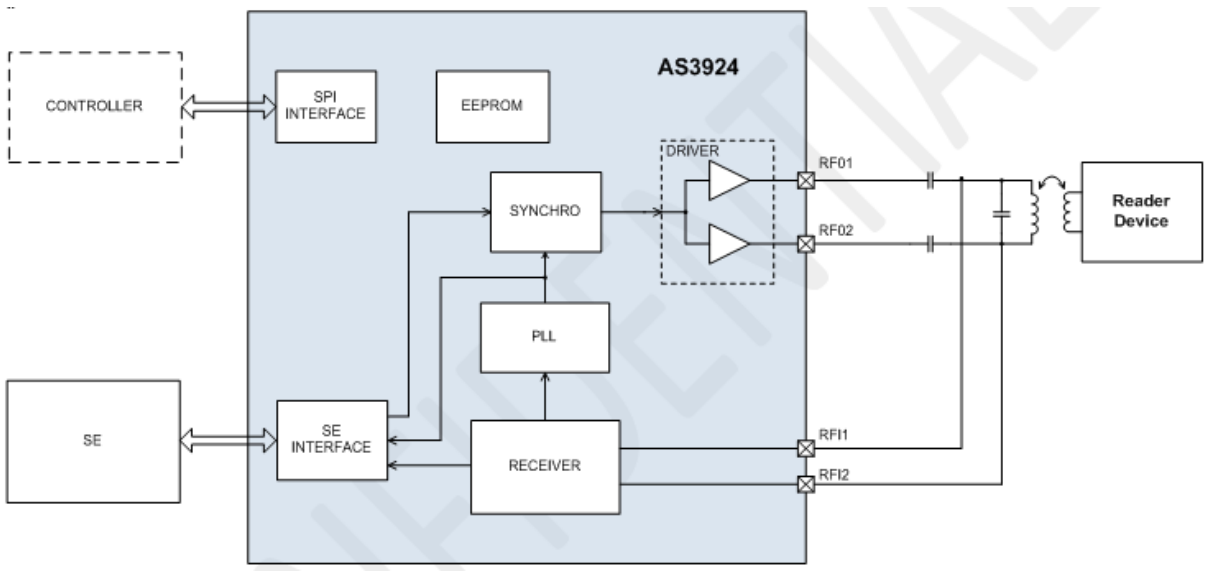

Figure 3: Simplified system diagram

Figure 4 shows the transmission one bit according to ISO14443 type A at 106 kb/s. Top canvas (1) depicts the signal on the reader antenna. Canvas 2 depicts the envelope of the signal on the reader antenna when the AS3924 transmitter is active. Canvas 3 depicts the current of the transmitter driver which is activated during the modulated periods of the subcarrier. The bottom canvas depicts the signal on the AS3924 antenna coil. Due to antenna Q factor the amplitude increases while transmitter is active (activation time is too short to reach steady state), when the transmitter is disabled the oscillation induced by transmitter is decaying. In the second half of bit period there is no transmission, after the signal induced by activation of transmitter completely decays, the signal induced by reader carrier signal is reinstalled on the card antenna.

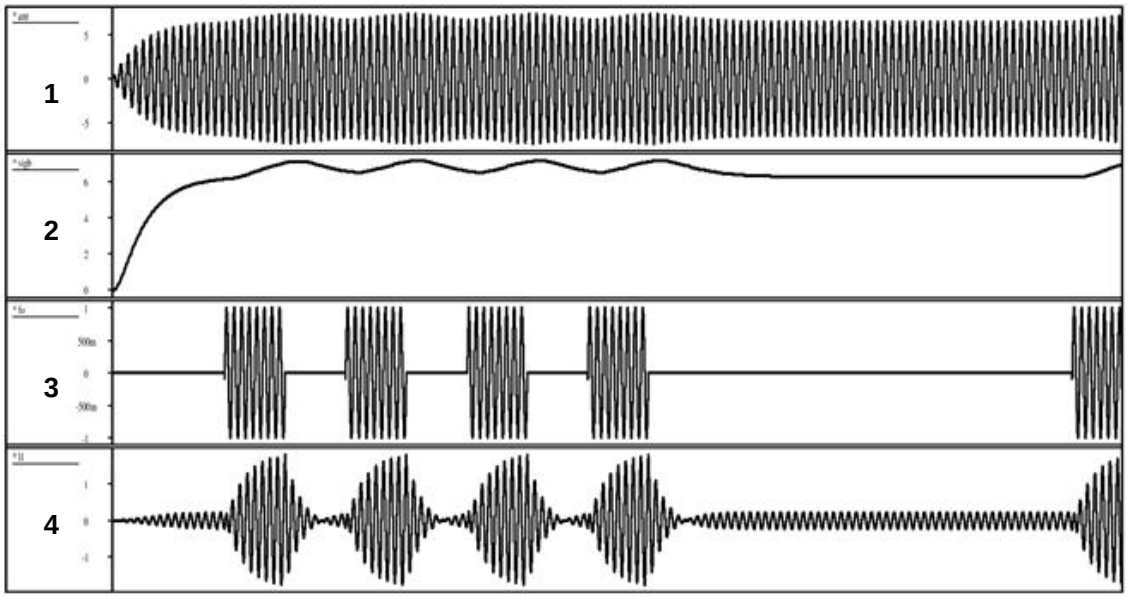

Figure 4: Example of ISO14443A 106kb/s transmission

4.1 Wake-up block description

The Wake-up block is a low power block used to detect the presence of a signal induced on RFI1 and RFI2 inputs. When the presence of a signal larger than the wake-up threshold is detected the frequency check block is activated.

In the absence of signal on RFI inputs, the AS3924 is in wake-up mode in which only this block is active.

AS3924 also features a special low power threshold mode in which current consumption is minimized. The intention of this mode is to support battery powered applications in which stand-by power consumption is a key parameter As in this mode the internal gain stage is not operating the threshold is relatively high, but still one order of magnitude lower comparing to passive load modulation ICs.

When the reader field is switched off, the wake-up block deactivates the AS3924 receive and TX blocks and sets it back to wake-up mode. The wake-up and deactivation thresholds have large hysteresis in order not to deactivate the operation by AM modulation of reader field.

4.2 Frequency Check block description

The Frequency Check block checks whether the frequency of signal present on RFI inputs is in 13.56MH frequency band. It compares frequency of the input signal to the internal clock frequency generated by an RC oscillator. It is enabled by the wake-up detector, in case the frequency check is successful the complete RX/TX system is activated.

The Frequency Check block is enabled/disabled by register. In low power wake-up threshold mode it is disabled.

4.3 Receiver block description

It provides the following functionality:

- input signal conditioning
- variable gain with AGC
- clock extraction
- peak detector (rectification)
- interface activation

This block amplifies the input signal, provides a clock signal extracted from the reader carrier frequency, and generates a signal which is proportional to input signal amplitude. It also puts the AS3924 back to Wake-up mode when the external field is deactivated. Depending on the application it can also define the DC operation point of the RFI inputs (applications using external AC coupling) and provides AC coupling of input signals (applications using internal AC coupling). Figure 5 depicts a block diagram of this block.

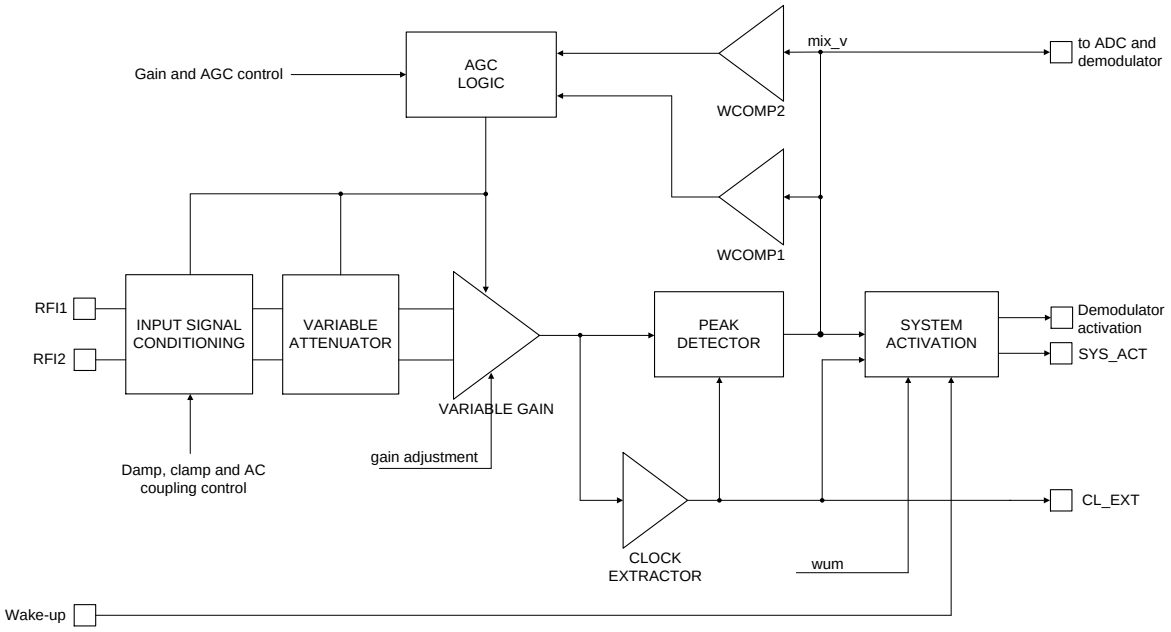

Figure 5: Receiver block diagram

RFI inputs are applied to the Input Signal Conditioning block which takes care of the biasing of the RFI input signal and decoupling of RFI inputs during AS3924 transmission. The next two stages provide variable attenuation and gain of the input signal. The output of the variable gain stage is fed to the Peak Detector and Clock Extractor.

The Peak Detector rectifies the input signal to provide an output signal (mix_v) which is proportional to the envelope of RFI1/RFI2 differential input signal. It uses a self-mixer concept where the Clock Extractor output is used as the clock. Signal mix_v is used for several purposes:

- It is used as an input to the AGC control loop
- It is used as an input to the Interface Activation block
- It is input to the demodulator, which detects the modulation superimposed on the reader carrier signal
- It is used as an input to the AD converter. ADC output value, combined with the info of actual gain setting, gives information about the input signal level.

A fast zero crossing comparator is used for clock extraction in order to keep phase delay as low as possible.

4.3.1 Input signal Conditioning

This block includes the following features:

- AC coupling of input signal
- DC biasing of RFI signal is case there is no DC path between RFO and RFI pins
- Input signal clamping during transmission in case external AC coupling is used
- Disconnect input to attenuation/gain stage during TX to keep its operating point
- Damping in case external AC coupling is not used in the application
- Antenna Q factor reduction in case RFI1 and RFI2 are directly connected to high Q antenna
- Blocking of input path in diagnostic modes

This block additionally contains a rectifier which generates a voltage which is used to bias the body of PMOS transistors used in switches (VAUX). This voltage can be observed through the AD converter for diagnostic and test purposes.

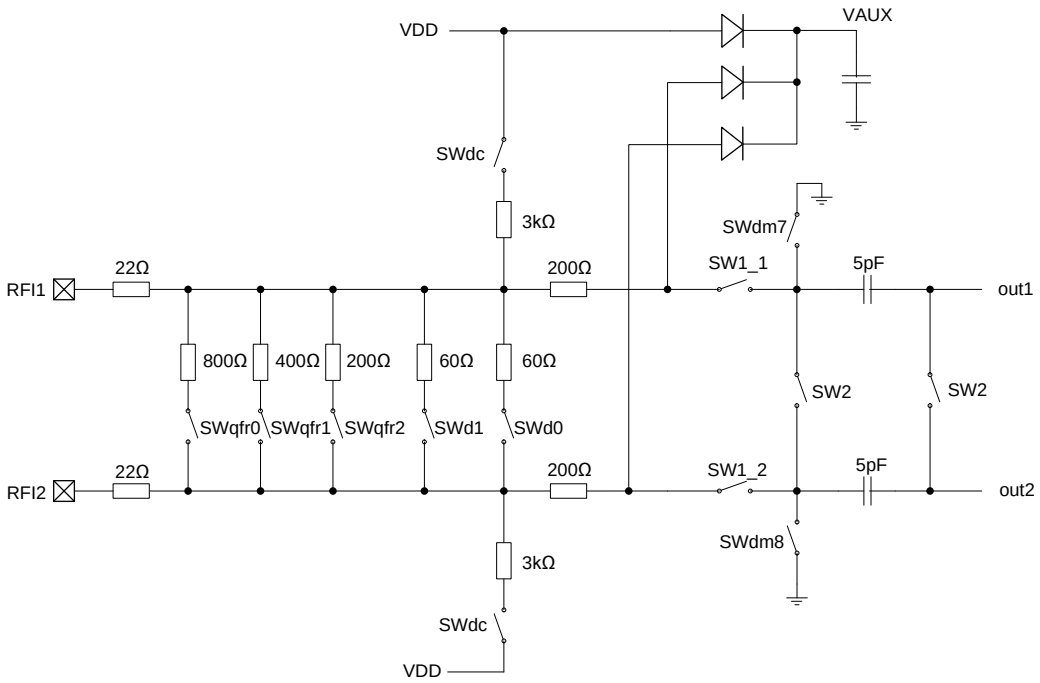

Figure 6: Input Signal Conditioning block diagram

4.4 Demodulator operation

The demodulator block detects modulation superimposed on the reader carrier signal which is used for reader to tag communication. The demodulator has to be able to demodulate Type A, Type B, and Type F modulation. The AS3924 can be configured to demodulate the carrier signal modulated according to any of the three supported protocols.

Type A signal is OOK modulated (100% ASK), while Type B and F use ASK modulation with modulation index ranging from 8% to 14% and 8 to 30%, respectively. Due to this, the AS3924 contains two parallel demodulators, an OOK demodulator for Type A and an ASK demodulator for Type B and Type F.

Both demodulators compare the instant value of the input signal envelope to reference voltages which are derived from the input signal using a certain time constant. The outputs of both demodulators are processed in a post-processing logic block.

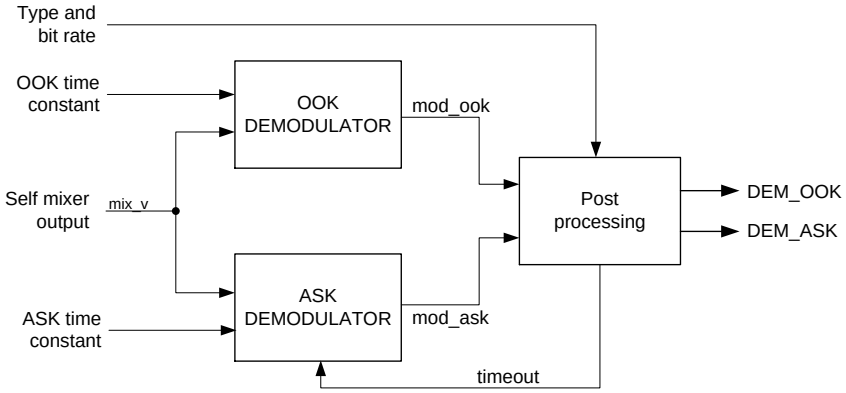

Figure 7: Demodulator block Diagram

4.4.1 ASK demodulator

Figure 8 depicts block diagram of the ASK demodulator. The mixer output signal is applied to a resistor divider which generates 105, 100, 96, 95 and 93% signals while mixer output is treated as 107% signal. The signal which is called 100% is directly applied to comparator input, while the other signals are used to generate the reference voltage (signal slow_ask). 105 and 107% are used to increase the reference voltage during the modulation state, while 96%, 95% and 93% are used to decrease the reference voltage during the non-modulated state. The later signal also defines the initial threshold as the reference settles to this level when a non-modulated level is present for a long time. As time constant of increasing and decreasing is the same the average value of reference sets in the middle between the modulated and non-modulated level of input signal. This concept has similar properties as AC coupled demodulator which is typically used for Type F demodulators as it greatly reduces the pulse width distortion in case of slow rise and fall times while it can also cope with Type B inputs signals.

The register settings define which combination of signal (higher and lower than 100%) is actually used to derive the reference voltage. Combinations 105-96, 105-95 and 107-93 are supported. The time constant of reference voltage is configurable for Type F and for Type B 106kb/s while it is fixed for higher bit rates of Type B.

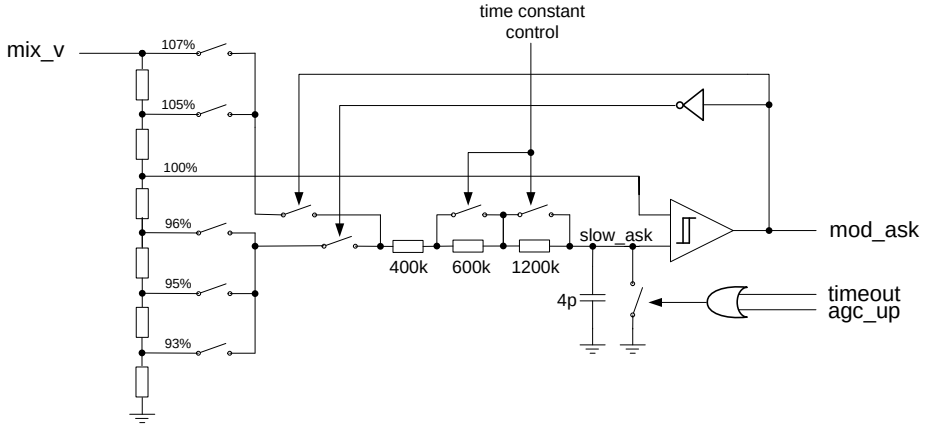

Figure 8: ASK Demodulator block Diagram

In case the input signal quickly drops (e.g. due to quick change of position in reader field) the ASK demodulator may stay stuck in modulated state. To mitigate this problem a time-out counter which intervenes if the modulated pulse duration is surpassing the maximum duration defined by the standard is added in post-processing block. In case duration of modulation pulse is longer that timeout value of this timer (113µs) discharging of the capacitor with the ASK reference voltage is initiated and lasts till the comparator switches to non-modulated state.

4.4.2 OOK demodulator

Figure 9 depicts block diagram of the OOK demodulator. The mixer output signal is applied to resistor divider which generates 100% signals while mixer output is treated as 107% signal. The signal which is called 100% is directly applied to comparator input, while the 107% signal is used to derive the reference voltage (slow_ook) during OOK modulation. The 100% signal is further divided by a resistor divider with several tap points which define the threshold options.

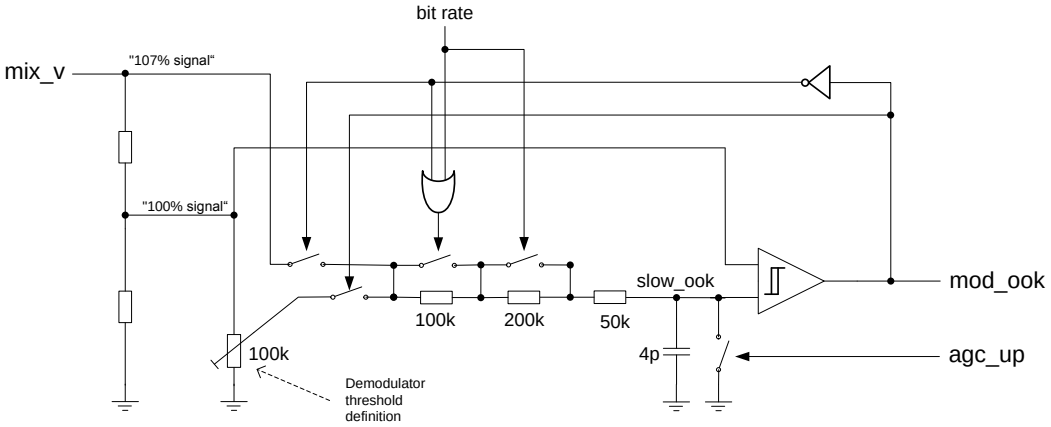

Figure 9: OOK Demodulator block Diagram

As the modulation pulses are shorter at higher bit rates, the time constant of the reference voltage varies with the bit rate which is currently used for PCD to PICC communication. *Table 1* lists the time constants which are actually used. During the modulation the 100kΩ resistor in the branch which defines the reference voltage is shorted to shorten the time constant. The input reference branch is connected to 107% signal to decay to a voltage which is slightly higher than the direct input to the comparator. This prevents false detection of end of modulation pulse which may happen when the field is off.

Table 1: OOK Demodulator voltage reference time constant

bit rate [kb/s]	Time constant [µs]
106	1.6
212	1.2
424	0.8
848	0.3

4.4.3 Post processing

The output of the ASK and OOK demodulators are shaped in the post processing blocks. The two outputs may contain spurious demodulated pulses which results from humps and overshoots which are superimposed to the reader field modulation pulses. Figure 10 depicts an OOK modulated pulse as defined by NFC Forum Analog Specification. The hump on the falling edge and overshoot on rising edge of modulation pulse are allowed.

In order to cope with humps and overshoots the post processing block contains timers which block the demodulator output transitions following the detection of falling and rising edges. These timers are adapted to selected RFID protocol and bit rate.

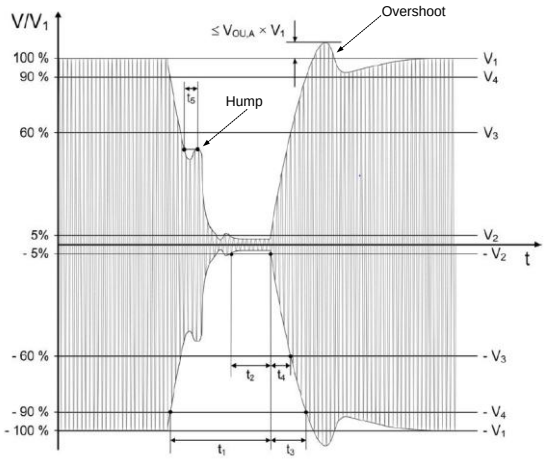

Figure 10: OOK modulation pulse (reproduced from NFC Forum Analog Specification)

In case of OOK modulation both demodulators detect the modulation pulse. As the threshold of ASK demodulator reference voltage is higher it generates a wider modulation pulse than OOK modulation. The ASK demodulator output is used to convey the modulation information on the RF_DATA_IO pin, while the OOK modulation is used to block the RF_CLK_RX during modulation. In order to keep the OOK modulation pulse inside the specification and to end the modulation pulse at the moment the clock pulse reappears on RF_CLK_RX the ASK demodulator output is forced low after the low to high transition of the OOK demodulator pulse. This is shown in Figure 11 where the post processing block outputs for an OOK modulated pulse are shown. The ASK demodulated signal is modified. Figure 12 depicts the case of ASK modulation where the modulated pulse transitions below the ASK reference but stays above OOK reference.

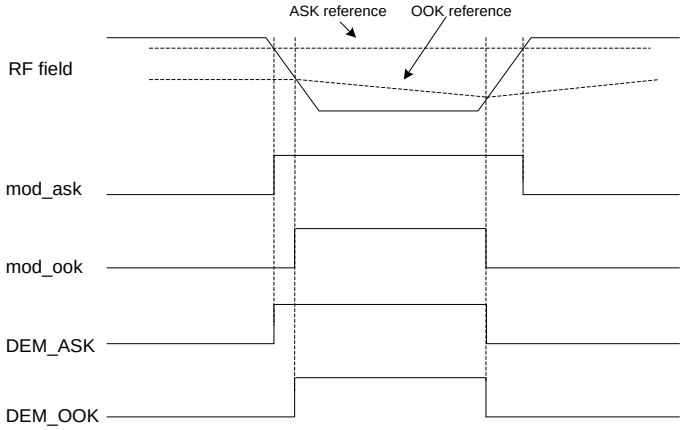

Figure 11: OOK demodulation

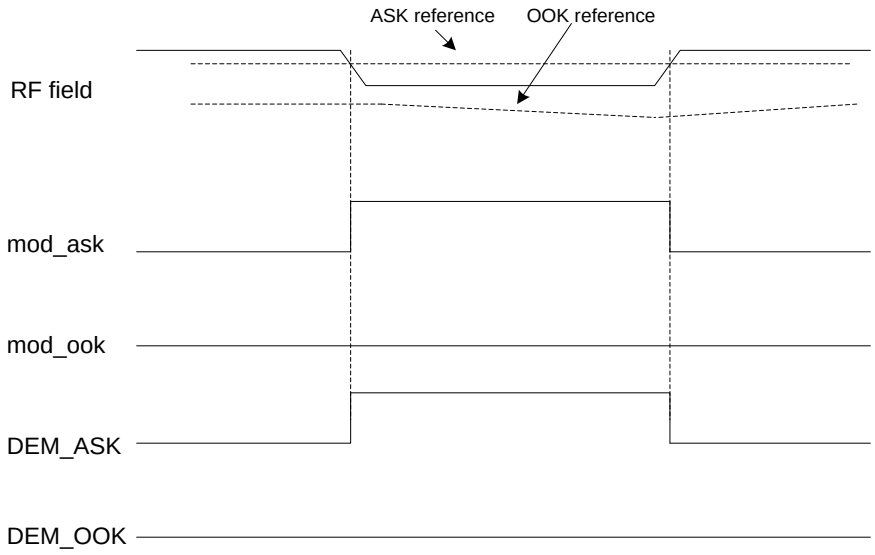

Figure 12: ASK demodulation

4.5 Interfaces to secure Element

4.5.1 ACLB Interface

The ACLB Interface acts as wired interface for connecting a contactless frontend (CL Frontend) of an IC with Contactless Interface (ICCI) to the AS3924. The intention of this interface is to reuse the ICs with existing contactless applications in environments which require improved operation range or smaller form factor antennas. The AS3924 acts as amplifier of incoming modulation which is superimposed on reader carrier signal and as transmitter of tag to reader communication.

The ACLB Interface is designed to support a contactless interface with maximum resonance capacitor of 30pF.

The ACLB interface contains two configurable push pull drivers. The push resistance to VDD is lower than pull resistance to VSS in order to avoid generating cross currents in the SE contactless interface.

The reader to tag modulation signal extracted by the receiver controls the ACLB. In case of OOK modulation ACLB is blocked, in case of AM modulation the output level is reduced.

ACLB is constantly monitoring the level of signal on its outputs in order to detect a drop produced by ICCI modulator switch during tag to reader communication.

Passive mode is a new feature on ACLB (see a separate chapter concerning this feature).

Figure 13 depicts a typical application where ICCI is connected directly to antenna coil to form a tag. Usually only a connection of antenna coil is necessary since resonant capacitor is already integrated in ICCI.

Figure 14 depicts application where the AS924 is used to “boost” performance of an ICCI. The AS3924 is placed between tag antenna coil and ICCI, ACLB interface signals are connected to ICCI contactless frontend.

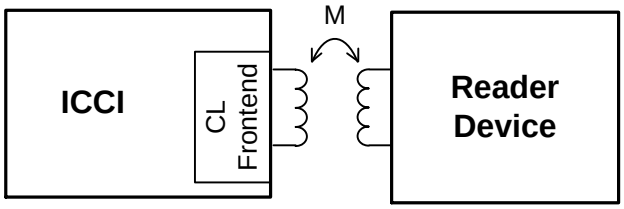

Figure 13: Example of ISO14443A 106kb/s transmission

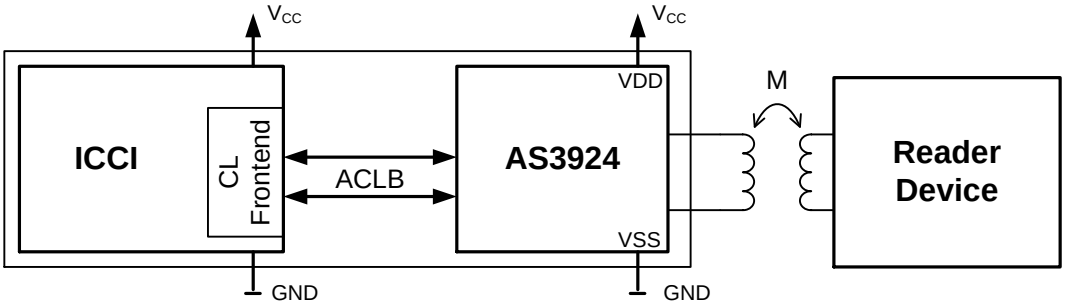

Figure 14: Application with AS3924 and ICCI

4.5.1.1 ACLB operation Principle

Figure 15 depicts connection of ACLB interface. ACLB signals ACLB1 and ACLB2 are connected to ICCI contactless frontend pins, which are usually named LA and LB. ACLB1 and ACLB2 are driven by push pull drivers which are driving reader carrier signal with opposite phases thus producing signals similar to those seen by ICCI contactless frontend in application depicted in Figure 14.

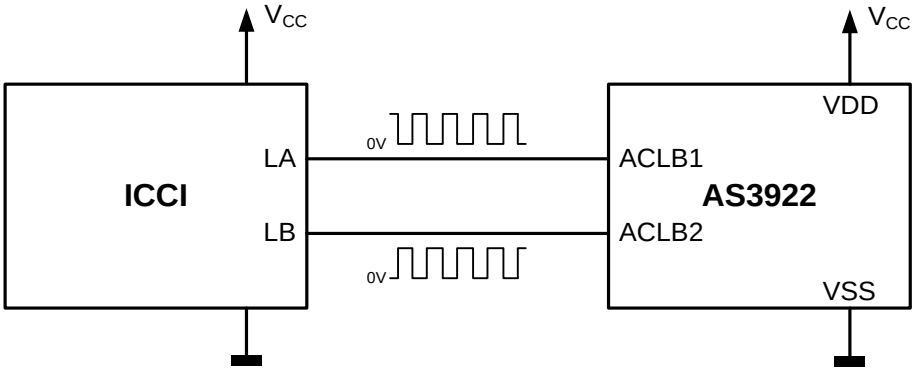

Figure 15: ACLB interface connection

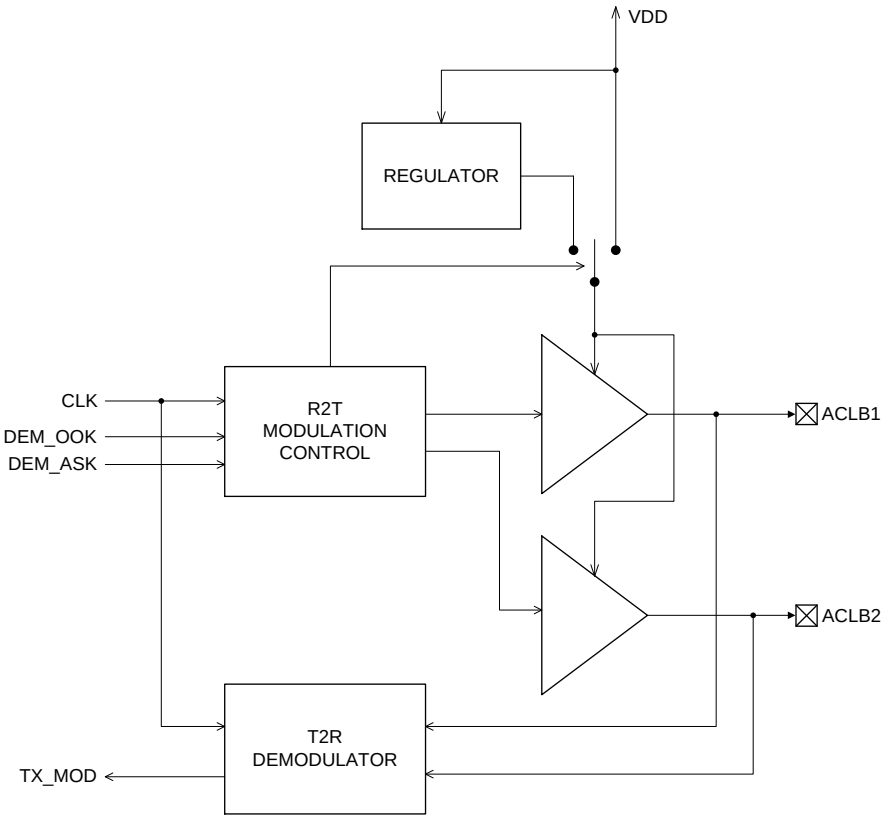

Figure 16: ACLB interface block diagram

Figure 16 depicts the ACLB interface block diagram. The main inputs are clock which is synchronous to reader carrier signal and output of the Demodulator. Clock signal is used to drive the two push-pull drivers while receiver demodulator output is used to superimpose the modulation of reader to tag communication to the ACLB signals.

ACLB drivers are composed of binary weighted segments where the resistance of path pulling to positive supply and resistance of path pulling to negative supply is separately adjustable by setting ACLB Driver Control Register.

The **Path pulling to negative supply** is composed of three segments, two can be enabled by settings in ACLB Driver Control Register, one is always connected. Typical resistance of segment which is permanently connected is 25Ω, typical resistance of MSB segment which can be enabled is 12.5Ω, while resistance of LSB segment is also 25Ω. Minimum resistance of path pulling to negative supply (both controllable segments are enabled) is therefore typically 6.5Ω

The **Path pulling to positive supply** is composed of switch which is used to perform AM modulations (see below) and driver resistance which is composed of six parallel segments which are all controlled by register settings. Typical resistance of switch is 14Ω, MSB segment of driver has resistance of 12Ω, while resistance of lower weight segments is binary increasing. Minimum resistance of path pulling to positive supply is therefore 20Ω (driver resistance in case all segments are enabled is 6Ω, resistance of switch is 14Ω).

Typical setting of ACLB driver resistance is such that the pull to negative supply is done with low impedance, while pull to positive supply is done with higher impedance, which is adjusted so that it is on one hand low enough to assure swing to VDD supply voltage and on the other produces an important voltage drop when the ICCI switches on its modulator switch for tag to reader communication.

Control of ACLB drivers and generation of reader to tag modulation is controlled by R2T Modulation Control block. The generation of reader to tag modulation depends on modulation type. In case of OOK modulation both drivers are kept at VSS while the modulated level is to be generated. ASK modulated signal (ISO14443B and FeliCa) is generated by switching the positive supply of ACLB drivers from VDD to output of internal regulator, which is configured so that the ration between VDD and regulator output voltage defines the ASK modulation depth. The regulated voltage and therefore ACLB reader to tag communication modulation depth is fully configurable via register settings.

T2R Demodulator block detects tag to reader modulation produced by ICCI and converts it in digital output signal which is used to control RFO drivers. This block is comparing the peak amplitude of ACLB1 and ACLB2 signals to internal reference which defined via register setting. In case peak amplitude is above this threshold the ACLB signal is considered non-modulated in case it is below this threshold it is considered modulated.

4.5.2 ICCI power supply

As mentioned before signals ACLB1 and ACLB2 swing between AS3924 negative and positive supply. Depending on AS3924 power supply and characteristics of ICCI this swing may not be sufficient to supply the ICCI through rectifier built in the ICCI contactless frontend. Due to this it is recommended that ICCI operates in so called mixed mode, where CL interface is only used for communication between the AS3924 and ICCI, while ICCI is supplied through its supply pins. Figure 17 depicts such configuration

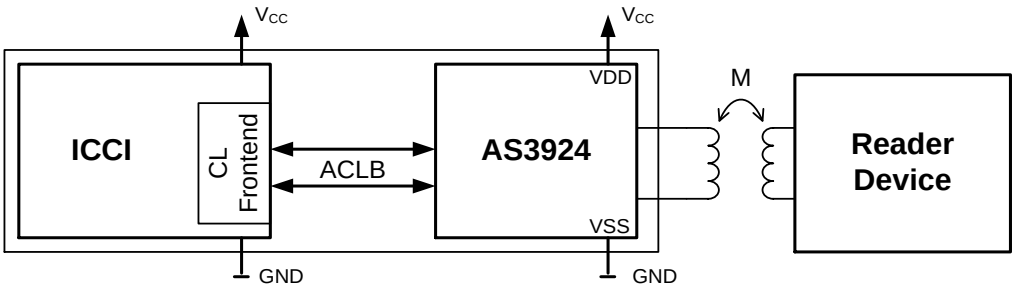

Figure 17: ACLB system architecture with separate power supply for ICCI

Disadvantage of power supply connection according to Figure 17 is that ICCI is always supplied and is therefore consuming current even when reader field is not present. In order to avoid this additional current consumption the AS3924 features pad VSP_SE_A with low resistance switch to VDD which can be used as positive supply of ICCI. This switch is switched on when the AS3924 detects presence of reader field. Additional advantage of using this switch is that the SE goes through power-up initialization every time the reader field is entered. Figure 18 depicts such configuration.

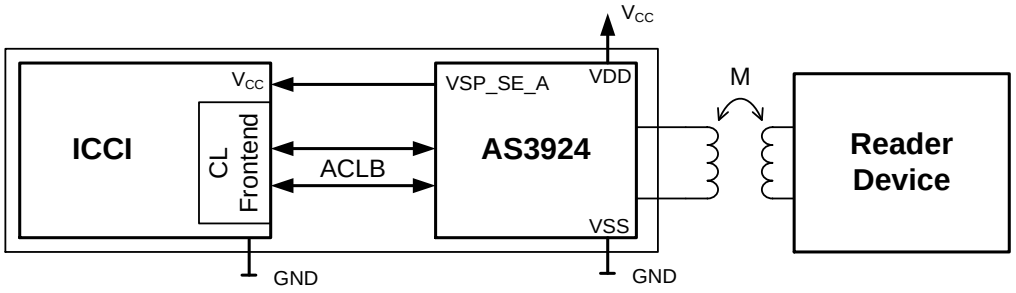

Figure 18: ACLB system architecture where VSP_SE_A is used to power ICCI

In case the ICCI does not feature positive supply pin it may be possible to also supply through ACLB. This is possible in case the VDD/VSS voltage swing created by ACLB is sufficient to create internal ICCI power supply which is larger than internal POR level. This necessary level differs from one ICCI to another, for certain ICCI it may also differ with temperature and process parameters. For such cases it is recommended to connect the ground of ICCI to system ground as depicted on Figure 19. Such connected avoids floating of ICCI die potential comparing to system ground.

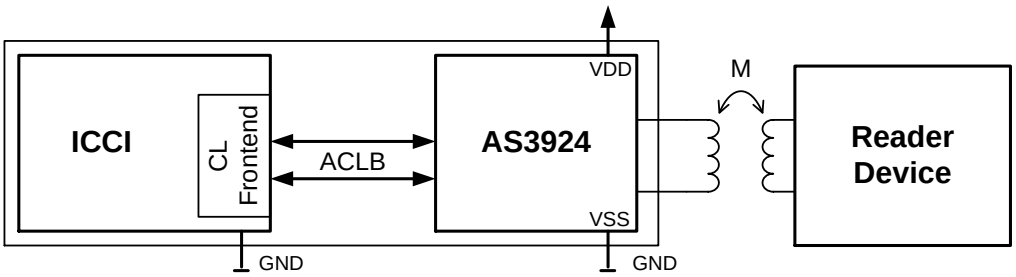

Figure 19: Recommended system architecture in case ACLB is used to power the ICCI

4.5.2.1 ACLB current consumption

The AS3924 ACLB is designed to drive ICCI with contactless frontend with maximum resonant capacitance of 30pF. Driving of this capacitive and additional resistive load of ICCI contactless frontend induces additional current consumption of several mA even in case ICCI is not supplied through ACLB. Current consumption due to capacitive load is equal to $2\times C_{CLF}\times VDD\times 13.56e+6$, which is 2.44mA at 30pF capacitance and 3V power supply. Current consumption due to parallel resistance is in the same range, which results in typical ACLB consumption during receive between 4mA and 5mA.

ACLB current consumption is increased during modulated periods of tag to reader communication due to additional current induced in ICCI modulator switch. This additional current consumption is in order of 10mA and may even be higher. Due to this it is very important to properly configure the AS3924 ACLB and ICCI modulator switch (in case some settings are available) to have on one hand reliable communication and on the other as low as possible current consumption.

4.5.2.2 Passive mode on ACLB

This feature allows a connection of large external antenna to ACLB pins to enable contactless operation of a reader directly to ICCI. The AS3924 ACLB1 and ACLB2 pins do not load an external voltage source connected to them and this enable a contactless communication directly to ICCI contactless interface under the following conditions:

- AS3924 supply voltages VDD, VDD_RF and VDD_IO are below POR level or the AS3924 is in power-down mode.
- Voltage forced to ACLB is in range from -0.3V to 5.5V

Note: ICCI CL interface has to keep the ACLB signals in range specified above.

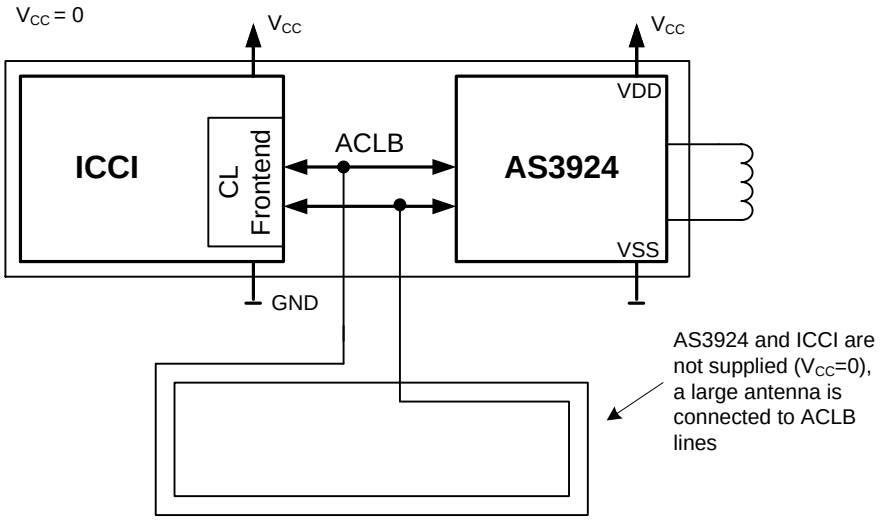

Figure 20: Passive mode on ACLB

4.6 Power Efficiency

This section summarizes the techniques implemented in AS3924 to reduce power consumption and improve its power efficiency.

4.6.1 RF Output impedance

The driver block (Figure 21 and Figure 22) is composed of two identical TX driver sub-blocks which contain 3Ω push-pull drivers and parallel driver which is active during damping. The TX driver sub-block is controlled by a logic block which controls the TX process including damping on the receiver input and auxiliary CDMP pins. The TX driver output resistance may be reduced to 2Ω. Some additional measurements to determine whether such change would be beneficial for performance are needed.

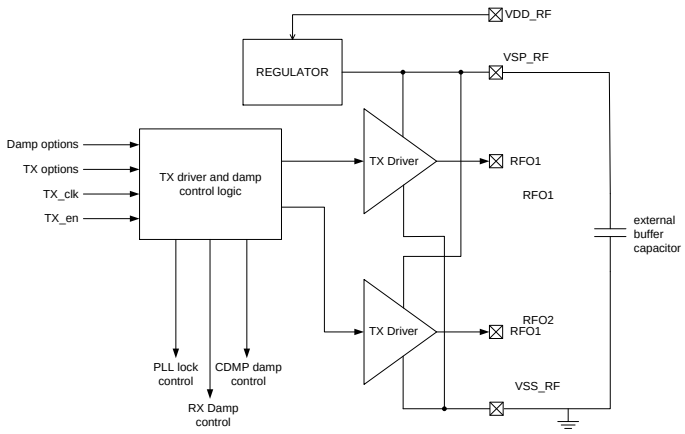

Figure 21: Antenna Driver

The default antenna driver mode is differential. In this mode the RFO1 and RFO2 drivers are driven in opposite phase; alternatively the output drive can be used in single drive mode, in that case the RFO driver may be either inactive or driven in phase with the RFO1. In the latter case the RFO1 and RFO2 pins may be shorted externally to result in 1.5Ω single driver.

Three modes which differ is state of drivers when transmission is not active are supported:

- one driver is high and the other is low (HL mode)
- both drivers high (HH mode)
- both drivers low (LL mode)

The preferred driver mode is the HL mode has to be used. Results of this mode will be a full differential signal at first transition. One of the last two modes has to be used in case there is a DC path between the two driver pins and/or between the driver pins and the RFI pins. In case of DC path between RFO pins and RFI pins HH option is preferred as it results in larger operating range of receiver (in LL configuration the RFI input signal is clamped by ESD protection diode connected to VSS).

Figure 22 depicts TX driver sub-block. It is composed of the main driver with a 3Ω push and pull branches and additional parallel driver with configurable output resistance which is used for damping. During damping the main driver is put in tristate (both branches are switched off) while the parallel damping driver continues to drive the antenna LC tank in order to dissipate the energy stored in the antenna LC tank. The damping resistance of the TX drivers is defined by register setting. For more details about damping please refer to chapter *4.7.*

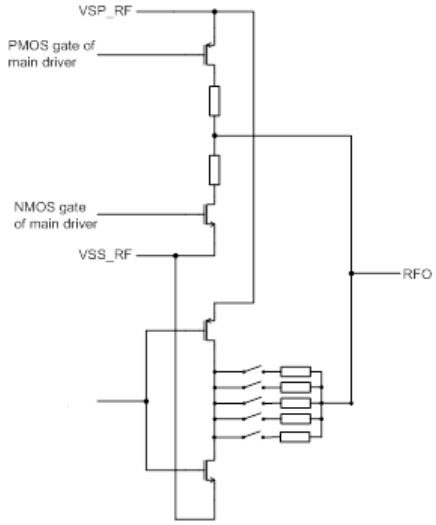

Figure 22: TX Driver block diagram

4.6.2 VSP_RF regulator

TX Drivers are supplied by the VSP_RF regulator. The output power may be controlled by adjusting the regulated voltage VSP_RF. The VSS_RF pin is the negative supply of the TX drivers. Externally it has to be connected to the same potential as the VSS pin (ground). The two pins are separated to assure a low impedance path from RFO pin to ground and to decouple the rest of the IC from perturbations generated by large current spikes generated on the RFO pins.

Two modes of setting the VSP_RF will be supported, “relative” and “absolute”. In “relative” mode the regulated voltages are scaled to VDD; in “absolute” mode the highest voltage is VDD, the send largest voltage is 2.4 V, while the others follow on 0.8 steps.

4.6.3 Wake-up including specific low power wake up

In order to save energy and enable transmission only in presence of an active PCD polling for PICC a special feature called “wake-up” will be implemented in the AS3924. The Wake-up is a low power block used to detect the presence of a signal induced on RFI1 and RFI2 inputs. When the presence of a signal larger than the wake-up threshold is detected the complete AS3924 RX/TX System is activated.

When no signal is present on RFI inputs and the AS3924 is in Wake-up mode, only this block is active. Several wake-up thresholds will be supported and configurable via register settings. The Wake-up Detector is a low power block with first order frequency selectivity from 1MHz to 25MHz (-3dB range).

Table 2: Wake-up Threshold variation

WU Threshold variation	*Activation range variation*
±50%.	*±14.5%*
±25%.	*±7.7%*
±20%.	*±6.2%*
±16%.	*±5.1%*

AS3924 also features a special low power threshold mode in which the gain stage is not operating. It is replaced by a rectifier output of which is connected to a simple inverter stage threshold of which is defined with MOS threshold. The intention of this threshold is to support battery powered applications in which power consumption is a key parameter.

4.6.4 Frequency check block

Before waking up the entire chip only based on wake up threshold, AS3924 checks the frequency of the signal to ensure it is a 13.56MHz signal. This reduces the amount of unwanted wake ups.

4.7 Damping and PLL lock delay

As already mentioned PLL has to be relocked from time to time while the reply frame is being transmitted. PLL can only be relocked once the oscillation built in the Antenna LC tank decays and the signal induced by reader field is restored. In several cases decay defined by antenna LC tank Q factor is too long and there is not enough time to synchronize the PLL. In such cases damping of antenna LC tank has to be used.

During damping the energy stored in all reactive elements in antenna LC tank is dissipated. Damping is mentioned in several chapters dedicated to AS3924 building block description, but the operating of the damping system refers to this chapter as a complete picture of damping can only be seen when the complete damping system is described. Parts of the damping system are incorporated in the Receiver, AUX Damp block and Antenna Driver.

4.7.1 Damping in case of BPSK AND TX mode

BPSK coding is used for communication for tag to reader in all ISO14443 modes except Type A 106 kb/s where Manchester code is used (see Figure 4 for example of Manchester code). In BPSK code, the subcarrier signal is always present; the difference between logic 1 and logic 0 signal is in phase of the BPSK signal. The number of subcarrier frequency

periods per data bit depends on bit rate (8 periods for 106kb/s, 4 periods for 212kb/s and 2 periods for 424kb/s). Figure 13 depicts an example of BPSK code. Signals in canvases are the same as in case of Figure 23. During normal subcarrier transmission, synchronization of the PLL is not possible since the signal on the LC tank is decaying during the period without transmission and reader carrier signal is not established by the end of this period. Synchronization of the PLL would only be possible during BPSK phase change where the time of non-modulated period during which the transmitter is not active is double (1.18us). Such case can be seen in Figure 23. The time during which the PLL could be synchronized is relatively short (about 0.6us), since the oscillation induced by transmitter has to decay first. Additionally the time between two phase shifts where synchronization could be done depends on data and can in worst case take place only once per data byte (worst case 86us). The combination of short synchronization time and long time between two synchronizations may lead to loss of phase synchronization between the carrier signal and transmitted signal and due to this an error in communication tag to reader.

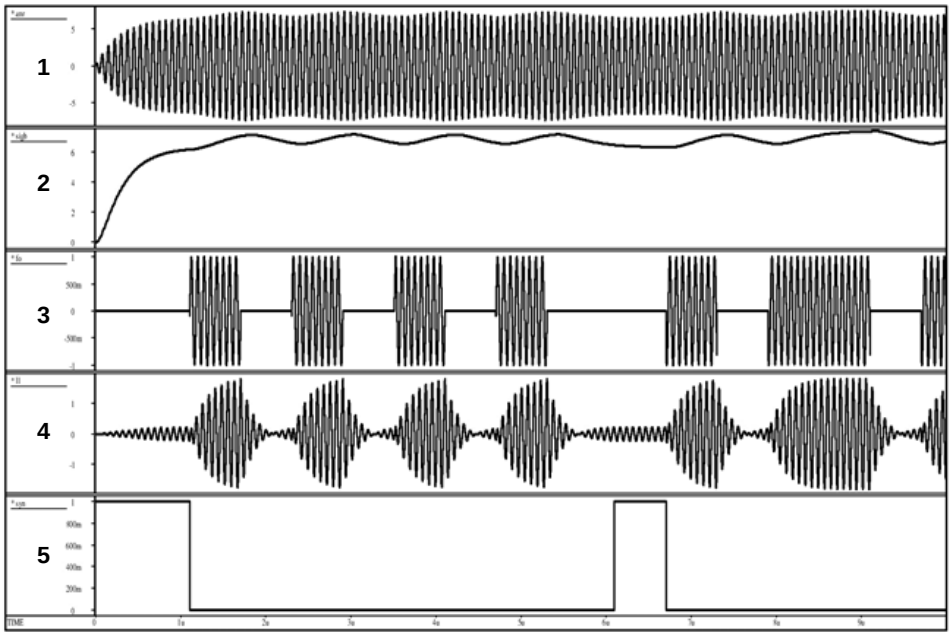

Figure 23: Example of BPSK code transmission

Since the cases where the non-modulated phase of BPSK signal has double duration are too rare to keep the PLL in phase, the only solution is to make resynchronization of the PLL during non-modulated phases of the subcarrier frequency of normal duration (8 periods of fc, ~0.59us). With such an approach the PLL resynchronization is done in most cases in every subcarrier period, in case of phase change where the modulated period is doubled this time would be increased to 1.5 periods. Resynchronization of the PLL is only possible after the oscillation built on antenna LC tank during modulation phase decays and the reader carrier signal is established again. Since decay of signal on the LC tank lasts several periods of carrier frequency (depending on LC tank Q factor), which does not let enough time for resynchronization, this decay has to be shortened. This can be done by reduction of the LC tank Q factor (damping) after the modulated phase during which the transmission is active. By doing this the energy stored in LC tank is quickly dissipated and the oscillation on the LC tank stops very quickly. Typical time during which Q factor is reduced to dissipate the energy stored in antenna LC tank is two to three periods of fc. This leaves five to six periods of fc to perform synchronization of PLL.

Figure 24 depicts the same sequence as Figure 23 this time with addition of damping and resynchronization in every non-modulated period of subcarrier. In this figure there are two logic signals in canvas 5. The bottom signal is high when the PLL is locked and synchronization is performed, the signal above is controlling the damping. When this signal is high - damping is active. The effect of damping is clearly seen in the canvas 4 where the oscillation on antenna LC tank stops practically immediately after the end of transmission. Once the damping system is switched off, the signal induced by the reader is restored and the PLL relock can be done.

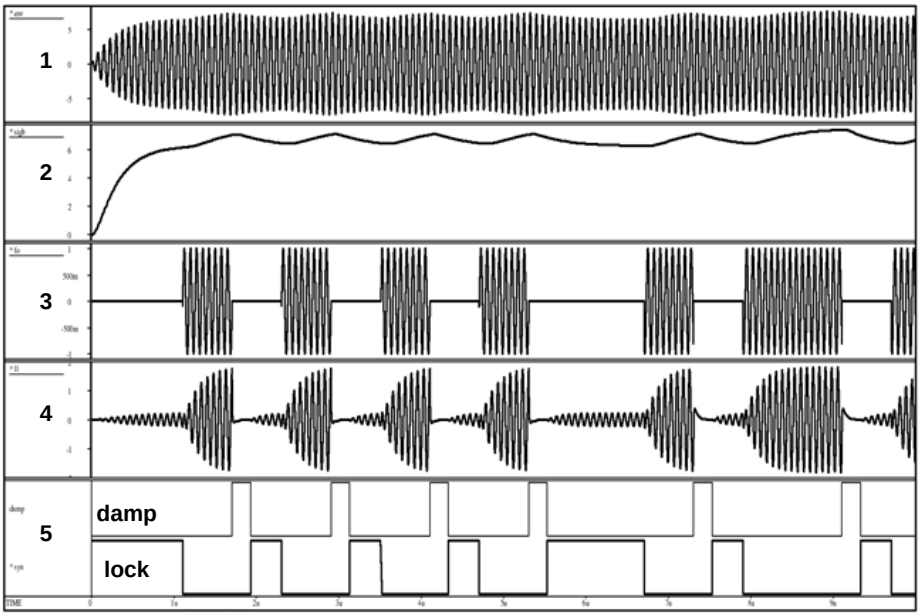

Figure 24: Example of BPSK code transmission with damping

Chapter 5 Operation mode and protocols

5.1 Transmission modes

Main transmission modes implemented to generate a tag reply is the:

- **AND mode**: Antenna is only driven during first state (also called modulated state 1 - MS1) of tag to reader communication. There is no transmission during second state

Given that active load modulation aims at enabling as small as possible antennae, it is believed that increasing as much as possible the load modulation amplitude through specific transmission modes is beneficial.

5.1.1 Support of Manchester code

Figure 25 depicts both transmission modes in case of ISO14443 Type A 106kb/s (Manchester code). During the parts of the code where there is no subcarrier signal there is no transmission.

IOT testing with AS39230 has shown that some readers have problems with receiving XOR TX mode in Type A 106kb/s. The reason for these problems may be in fact that during silence phase (period without subcarrier) there is no transmission which in creates another transition on reader. One possibility to mitigate this problem is to move the last transition in the period without subcarrier. In that case reader would see another transition later in the silence phase of Manchester code which it may neglect (interpret as a noise spike). This can be done by setting TX Type Control Register bits *xor_man1* and *xor_man0* which extend duration of last MS2.

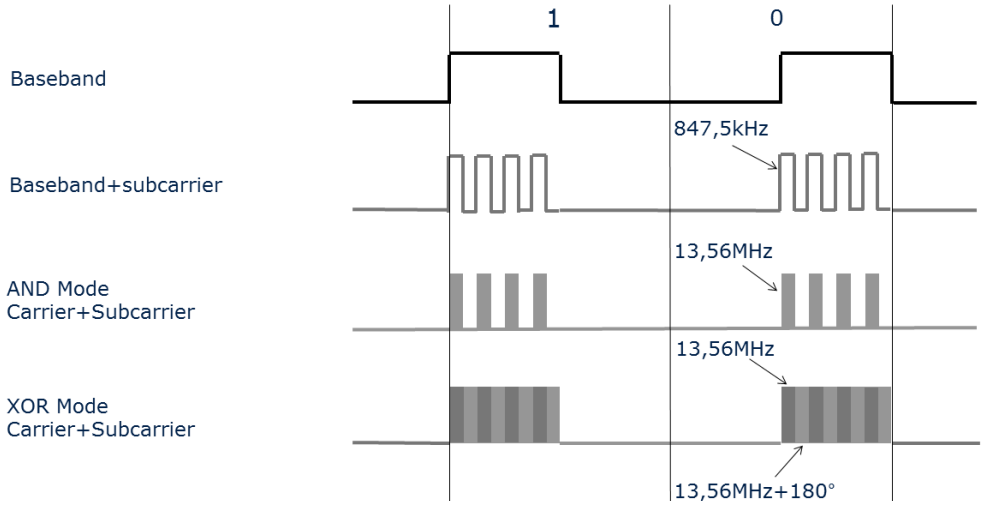

Figure 25: Transmission modes in case of ISO14443 Type A 106kb/s

5.1.2 New modes to support BPSK

New XOR transmission modes will be in AS3924 for Matthew project that will enable XOR transmission mode for high baud rates and BPSK.

The Figure 26 below provides a functional description of those new XOR modes.

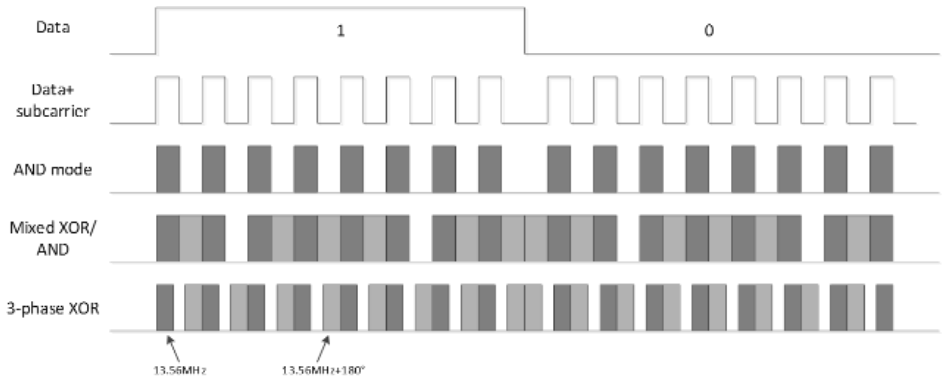

Figure 26 - New XOR modes implemented for BPSK and high baudrate

5.2 Special Modes during operation / transmission

5.2.1 Automatic Antenna Tuning (AAT)

The antenna coil inductance and Q factor are modified in presence of metal or other conductive material (like batteries for example). Typical AS3924 applications in the Matthew system are microSD and micro/nanoSIM cards having additional HF tag functionality. Environment of microSD and micro/nanoSIM slots differs from one mobile phone to another and they may affect antenna coil properties.

The AS3924 implement a special feature, the Automatic Antenna Tuning (AAT), which automatically adjust the resonance frequency of the antenna in order to achieve stable performances in within a well-defined range of boundaries conditions.

AAT is done by external voltage controlled variable capacitor, value of which is controlled by the AS3924 pin ATN (see Figure 27 for typical application schematics).

The AAT tuning procedure is automatically started after power-up initialization or triggered by sending a direct command AAT.

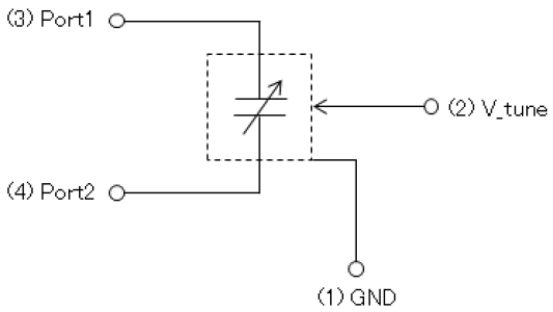

Figure 27: Schematic of variable capacitor (reproduced from Murata documentation)

5.2.2 Automatic Power Control (APC)

RFID readers are designed to handle a certain range of signal induced by tag reply. In case of low level signal the reading distance is limited by sensitivity of receiver, whereas in case of high level side it is limited by saturation of receiver gain stages. Using passive load modulation a large tag signal induced on reader is usually not a limiting factor for tag to reader communication. In case of tag reply generated by active transition technology it may generate high signal level on the reader LC tank and cause receiver saturation.

The AS3924 will include a special feature in order to control level of modulated signal. The function is the Automatic Power Control (APC) feature which is capable of reducing output power as function of input signal amplitude. This function will allow to cope with reader saturation problem above mentioned (signal is reduced in case of high coupling level between PCD and PICC and increased in case of low coupling condition).

The APC is acting on the driver stage of the AS3924 reducing the output level and consequently reducing the power consumption of the device. This function will allow to save power and increase battery life of mobile device.

5.3 System parameter exchange system via ACLB

The concept of this system is based on property of RFID communication where reader and tag exchange communication frames. Two communication frames of the same type (tag to reader for example) one after the other are not possible. RFID protocols require a minimum delay time between a frame sent by the reader and reply frame sent by the tag to be respected. In case ICCI sends a reply frame during this minimum delay time it is interpreted by the AS3924 as information which is not meant for transmission.

System parameter exchange over ACLB after PCD will operates in the following way:

- After every detected rising edge of reader modulation the AS3924 opens a window (Configuration Indicator Window) in which it can detect a modulation produced by the ICCI (Configuration Indicator Pulse). This window is opened from 16/fc (1.18µs) to 960/fc (*7.5×128/fc* ~ 70.8µs, same as T_{RXE}) measured from last rising edge of reader to tag modulation (it is 944/fc wide).
- Configuration Indicator pulse indicates to the AS3924 that two additional frames will be transmitted by the ICCI. The first frame is the Configuration Frame which contains the AS3924 configuration information and is not transmitted by the AS3924; the next frame is response frame which is transmitted. After response frame is transmitted new configuration setting defined in configuration frame are applied.
- Minimum time between Configuration Indicator and Configuration Frame is 5µs. Minimum time between Configuration frame and Response frame is also 5µs

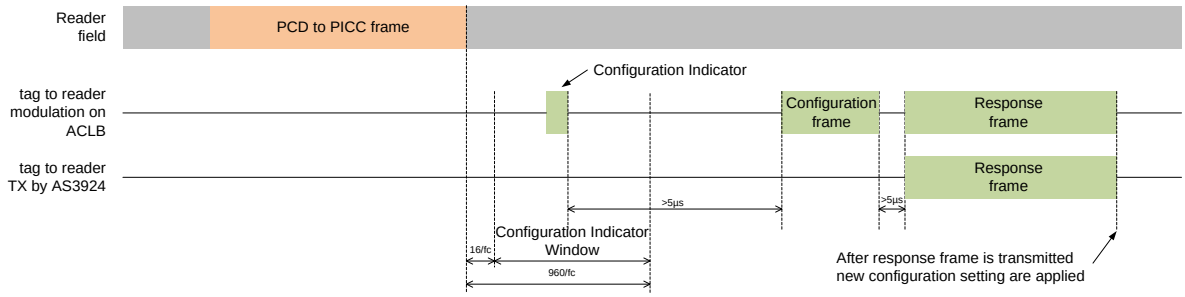

Figure 28: Case where Configuration Frame and response frame are sent by ICCI

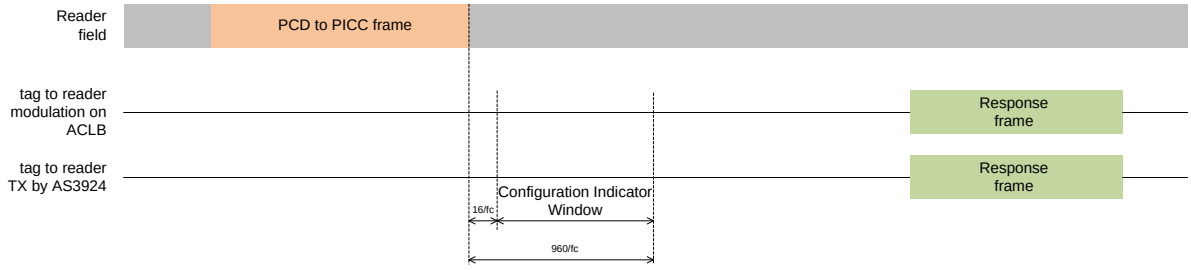

Figure 29: Case where only response frame is sent by ICCI

5.3.1 System parameter exchange at field-on

When it is enabled the AS3924 expects to receive a Configuration Indicator after the Initial Blocking timer expires, but not later than 4ms after activation of ACLB. As in case of configuration after PCD frame a Configuration Indicator followed by Configuration Frame has to be sent by ICCI. The AS3924 TX and RX are blocked until the end of configuration frame or till 4ms timeout after ACLB activation expires (in case configuration frame was not sent).

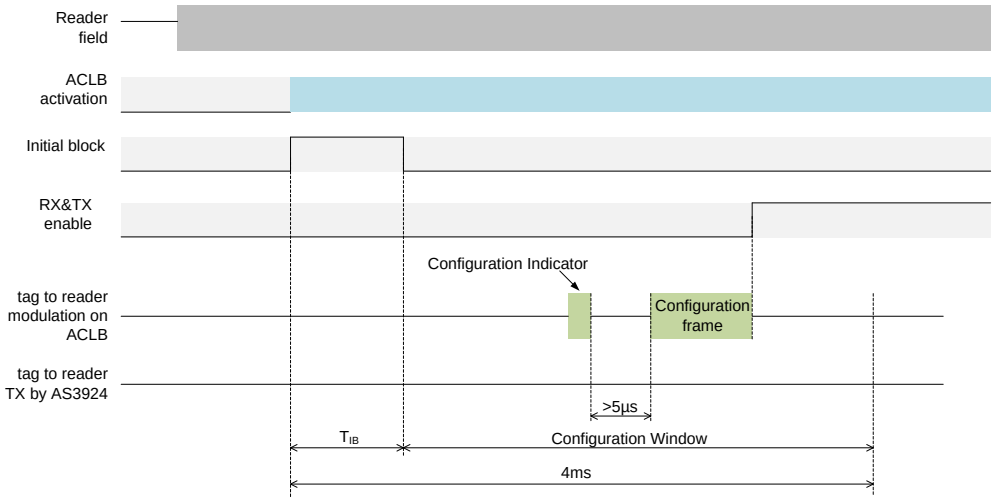

Figure 30: System parameter exchange at field-on

Chapter 6 List of Abbreviations

ALM	Active Load Modulation
AAT	Automatic Antenna Tuning
ACLB	Advanced Contactless Bridge
ADC	Analog Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying: modulation scheme
CL	Contactless
HF	High Frequency
ICCI	Integrated Circuit with Contactless Interface
NFC-WI	Near Field Communication Wired Interface
OOK	On-Off Keying: modulation scheme
PCD	Proximity Coupling Device
PICC	Proximity IC Card
PLL	Phase-Locked Loop
RFID	Radio-Frequency Identification
SE	Secure Elements
SPI	Serial Peripheral Interface
VCO	Voltage-Controlled Oscillator

Chapter 7 Bibliography

[1] RFID Handbook – Klaus Finkenzeller – Wiley